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DEFENCE RESEARCH CENTRE SALISBURY
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## TECHNICAL MEMORANDUM

ERL-0154-TM

A FAST, HIGH VOLTAGE, AVALANCHE TRANSISTOR Q SWITCH DRIVER

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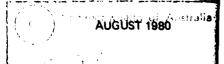
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TECHNICAL MEMORANDUM

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A FAST, HIGH VOLTAGE, AVALANCHE TRANSISTOR Q SWITCH DRIVER.

SUMMARY

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This paper describes the development of a fast high voltage switching circuit using avalanche transistors.

The circuit was found eminently suitable for Electro-Optic Q Switching and cavity dumping of lasers.

Many transistor types have been used to drive Q switch elements but in most cases the avalanche chain must be carefully matched to the load.

The circuit described here used the transistor type 2N5192 which was found to have a wide operating range thus allowing the chain to be easily matched to the Q switch voltage requirements. In addition it has proven very robust and not easily damaged by over voltage.

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## TABLE OF CONTENTS

		Page 1	No.
1.	INTRODUCTION	1	
2.	THE SELECTION OF A TRANSISTOR	1	
3.	THE AVALANCHE CHAIN	3	
	3.1 Voltage rise time	3	
	3.2 Optical switching speed	6	
4.	ALTERNATIVE CIRCUIT FORMS	7	
	4.1 Q switch circuit	7	
	4.2 Cavity dump drive circuit	7	
	4.3 Pulse gating	7	
5.	CONCLUSION	8	
	REFERENCES	9	
	LIST OF TABLES		
1.	AN ASSESSMENT OF TRANSISTORS IN THE AVALANCHE MODE	2	
2.	THE EFFECT OF A CAPACITIVE LOAD ON A SINGLE TRANSISTOR	4	
3.	THE EFFECT OF A CAPACITIVE LOAD ON A 6 TRANSISTOR CHAIN	5	
4.	THE EFFECT OF A CAPACITIVE LOAD ON A TIGHTLY PACKED CHAIN	6	
	LIST OF FIGURES		
1.	Test circuits for Avalanche transistors		
2.	2N2222 Avalanche characteristics		-1
3.	2N5192 Avalanche characteristics  Accession		

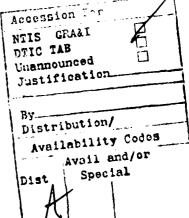
4. Avalanche transistor chain

7. Circuit for pulse output

8. PTM Q switch drive circuit

5. Equivalent circuit in ON state

6. Voltage step for 6 transistor chain



#### 1. INTRODUCTION

The WRELADS laser system being developed in the Electronics Research Laboratory requires a high repetition rate laser delivering pulses of 5 ns FWHM. As part of a study on lasers to meet this requirement, the Pulse Transmission Mode (PTM) laser was examined. In this mode, the laser cavity is closed with 100% reflecting mirrors at both ends. The laser is electro-optically Q switched in the normal manner then when the energy density in the cavity reaches its peak, the Q switch is shut very quickly. The energy drains from the cavity via the polarising prism in the time it takes to make one round trip of the cavity. Short pulses can therefore be produced fairly easily. To operate the Q switch in this manner requires two high voltage switching operations in which the first need only be short compared to the pulse evolution time (of the order of 50 ns) whilst the second needs to be considerably faster, ideally less than the time for one round trip of the cavity (2d/c, where d is the cavity length).

Hook et al(ref.1,2) investigated this method of operation using gas filled Krytron tubes for the witching. The circuit reported by them(ref.2) was used here but our version was found to be unreliable in operation. The results obtained by Hook et al were for a fairly long Q switched pulse (60 ns). Triggering in the circuit was performed optically with a high voltage vacuum photodiode sensing the leading edge of the Q switch pulse. For a symmetric Q switched pulse, approximately 30 ns are available in which to achieve switching at the peak of the pulse. If the Q switch pulse is short, say 20 ns, then the Krytron triggering delay of 20 ns is unacceptable as triggering would occur too late. In addition the life of the Krytron was not expected to exceed 10<sup>5</sup> firings.

For these reasons the Krytron was not considered suitable as a switch for our application. However Ley et al(ref.3), had used avalanche transistor chains to provide the fast, high voltage ( $\cong$ 1 kV), trigger pulse to a Krytron. By using more transistors in the chain, it was decided that one could use the avalanche device in place of the Krytron.

#### 2. THE SELECTION OF A TRANSISTOR

A literature survey established that many authors had used transistors in the avalanche mode(ref.4 to 7) but there seemed to be no clear reasons for a particular choice of transistor type. The course followed was to procure those transistors referred to in the literature together with a wide selection of other transistors which were readily available and test them all in suitable test circuits.

Good background information on avalanche switching is available in the Motorola Switching Transistor Handbook, a Ferranti publication titled "The Use of Transistors in the Avalanche Mode" and various articles(ref.8 to 11), most of which were published in the early 1960's.

A simple test circuit, figure 1(a), was built to test each transistor individually. A 5 V pulse was applied at the input to the base and the voltage across the transistor was increased until it began to fire. This voltage was noted as the lower working limit. The voltage was then increased further until the transistor went into a free running avalanche, erratic and untriggered. This was noted as the upper voltage limit.

In Table 1, a list of transistor types tested is shown, together with approximate lifetimes and upper and lower voltage limits. From an examination of the properties of the transistors listed a selection was made and larger quantities of the more promising types were obtained and subjected

to more extensive testing.

TABLE 1. AN ASSESSMENT OF TRANSISTORS IN THE AVALANCHE MODE

Туре	Upper voltage range	Lower voltage range	Approximate rise time (ns)
AX6101	142	86	2.0
AX8001	139	92	1.8
BFY50	125	100	1.5
MPS6520	122	84	1.5
SE4010	193	124	1.7
ZTX300	115	79	1.6
TT3642	102	93	1.4
i			
2N697	147	97	1.7
2N910	132	97	1.8
2N1482	212	172	2.0
2N2102	208	202	1.8
2N2218	101	99	1.5
2N2222	116	88	1.7
2N2405	176	125	2.6
2N2484	137	124	1.7
2N2714	133	83	1.5
2N3019	175	140	
2N3055	1 <b>6</b> 5	160	
2N3503	199	159	1.5
2N3565	196	112	2.1
2N3568	160	144	1.7
2N3569	179	124	1.6
2N3641	195	183	1.7
2N3643	128	85	1.4
2N3694	130	92	2.5
2N3707	118	103	1.7
2N3904	105	92	4.2
2N3923	334	242	5.0
2N4300	160	132	2.2
2N4400	103	65	1.8
2N4922	262	163	4.0
2N5192	211	142	2.0
<u> </u>			

One characteristic not measured by the circuit of figure 1(a) is the voltage drop across the transistor in the ON state. To measure this a test circuit as in figure 1(b) is helpful. A pulse forming network is used to give a long pulse (#200 ns) so that fast transient voltages can subside and allow the ON voltage to be read on an oscilloscope free of interference.

The results of further testing are shown in the histograms of figures 2 and 3 for two transistor types. Figure 2 is for the 2N2222 transistor used by some workers. Note that its characteristics show a fairly wide spread. In addition, if the upper voltage limit were exceeded the transistor was often irreversibly damaged. Figure 3 shows the results for the transistor finally selected, the 2N5192. It has a high operating voltage, a wide operating range and was found to be very robust, ie it is not easily damaged by over voltage. This transistor had previously been used by Mr V.D. Woolley of this group, as a driver for a light emitting diode in the avalanche mode.

Using the circuit of figure 1(b), the ON voltage for the 2N5192 was found to be  $\cong 20~\mathrm{V}$ .

#### 3. THE AVALANCHE CHAIN

The avalanche chain is essentially the same as that used by Ley et al(ref.3) and is shown in figure 4. A small capacitor across the bottom (triggered) transistor was used to increase the reliability of triggering. Note that the accessible switched voltage at the emitter of the top transistor is less than the full supply voltage due to the dividing action of the resistor chain. Resistor  $R_{\gamma}$  may be smaller than the others in the chain but it

limits the current in the ON state and cannot be reduced too far or the transistors will latch on causing certain failure. For the 2N5192 the latching current was found from the circuit of figure 1(a) by reducing the resistance gradually until latching occurred. The test can only be done once on a transistor because it damages the device. Although the power dissipation may be less than the rated power when operated in the normal mode, the avalanche action occurs in small "plasma" columns and the localised heating is excessive. Latching current for the 2N5192 is approximately 10 mA.

For a KD\*P Q switch, having a quarter wave retardation voltage of 3.8 kV at 1064 nm, a chain of 20 transistors is required. From the histogram data of figure 3, the chain would operate between 3.2 kV and 4.5 kV, thus allowing some adjustment either side of the nominal quarter wave voltage.

#### 3.1 Voltage rise time

An equivalent circuit for the chain is shown in figure 5 with a capacitive load (C) and stray inductance ( $L_s$ ). The chain is assumed to have a source

resistance  $R_{_{\rm S}}$  in the on state. The effect of stray inductance is to

generate a back e.m.f. opposing the voltage change across the capacitive load of

$$V = L_s \frac{di}{dt}$$

The circuit will ring at a frequency of

$$w^2 = \frac{1}{L_s C}$$

from which the stray inductance can be obtained as

$$L_s = 1/\{(2\pi f)L2C\} = (T_c)^2/(4\pi^2C)$$

where  $T_{c}$  is the period of the ringing cycle.

A typical result is shown in figure 6, the rise time and ringing cycle are shown for a tightly packed 6 transistor chain with a 1000 pF load.

The voltage rise time is

$$\tau$$
 = 26 ns  $(10\% - 90\%)$ 

and the period of the ringing cycle is

$$T_{c} = 56 \text{ ns}$$

giving

$$L_s = 0.079 \mu H$$

It was further noted that the rise time was directly related to the ringing cycle period. The mean over 23 readings gives

$$\tau_{v} = 0.45 T_{c}$$

Table 2 gives the measured results for a single transistor, with no attempt to minimise stray inductance. The last figure in the table is for a 1000 pF capacitor connected with short leads directly across the transistor. This should be compared to the first figure giving the result for a 1000 pF capacitor with its leads intact. A significant reduction in stray inductance could be made with short leads.

TABLE 2. THE EFFECT OF A CAPACITIVE LOAD ON A SINGLE TRANSISTOR

Capacitor C	Rise time T	Ringing cycle period T	τ ··· Τ	Stray inductance L s
(pf)	(ns)	(ns)		(HH)
1000 470 330 220 150 82 47 1000	36 28 20 16 14 12 9	80 52 44 38 29 26 19	0.45 0.54 0.45 0.42 0.48 0.46 0.47	0.162 0.146 0.149 0.164 0.142 0.209 0.195 0.0082

\* Short leads

Table 3 gives the results for a 6 transistor chain, again with no attempt to minimise stray inductance. The rise times are longer and stray inductance higher than for the single transistor. The last figure in Table 3 was obtained when the current rise was limited by a resistive load of 1 K $\Omega$  in series with the capacitance as shown in figure 7. The effect of the load resistor is to limit the rate of rise of the current and hence the back e.m.f. The voltage appearing across the load resistor is a fast pulse. For the pulse to be nearly equal in amplitude to the switched voltage, the load resistor should be large compared to the source

resistance. Best results were obtained when the time constant produced by the capacitor and resistor was

 $\tau = RC = 200 \mu s$ 

TABLE 3. THE EFFECT OF A CAPACITIVE LOAD ON A 6 TRANSISTOR CHAIN

Capacitor C	Rise time <sup>T</sup> v	Ringing cycle period T	t v T	Stray inductance L s
(pf)	(ns)	(ns)		(µH)
1000 470 330 220 150 82 47 1000	48 30 26 22 16 14 10 8	106 76 60 50 38 31 25 None	0.45 0.39 0.43 0.44 0.42 0.45 0.40	0.28 0.31 0.28 0.29 0.24 0.30 0.34

\*

Table 4 gives the results for a 6 transistor chain which was tightly packed in an attempt to minimise stray inductance. Comparison with Table 3 shows that the stray inductance was reduced by a factor of 4. The last figure of Table 4 indicates a stray capacitance of 17.8 pF using the mean inductance to calculate the capacitance. This is considerably higher than the nominal capacitance of the high voltage probe (3 pF) used for the measurements. Hence the probe did not unduly influence the results.

<sup>\*</sup> with 1  $K\Omega$  limiting current

TABLE 4. THE EFFECT OF A CAPACITIVE LOAD ON A TIGHTLY PACKED CHAIN

Capacitor C	Rise time T	Ringing cycle period T	τ - <u>Υ</u> Τ <sub>c</sub>	Stray inductance <sup>L</sup> s
(pf)	(ns)	(ns)		(HH)
1000 470 330 220 150 82 47	26 17 14 12 9 8 6	56 38 30 25 18 15 11	0.46 0.45 0.47 0.48 0.5 0.53 0.55	0.079 0.078 0.069 0.072 0.055 0.070 0.065

\* Probe and stray capacitance only

For Q switching, no special care is needed to eliminate stray inductance as voltage rise times of 8 ns are easily obtained with a resistive load to limit the current. This is much less than pulse evolution times (50 to 100 ns) as required.

For pulse gating or cavity dumping, where a fast high voltage pulse is required, some effort to minimise stray inductance is needed but even here the effects of capacitive loading are minimised by the resistive load across which the fast pulse is developed.

## 3.2 Optical switching speed

Although the voltage rise times given in Tables 2 to 4 are not better than 8 ns, the optical switching is faster. The transmission of the Q switch as a function of time is

$$T(t) = \sin^2 \{(\pi.t)/(2.t_v)\}$$

where  $T(t) \quad \text{is the transmission as a function of time and } \tau_{_{\boldsymbol{V}}}$  is the voltage rise time.

For the transmission to change from 10% to 90%

$$\tau_{T} = 0.58 \tau_{V}$$

where  $\tau_{_{\rm T}}$  is the transmission rise time.

With  $\tau_V$  = 8 ns, the transmission rise time is

$$\tau_{\rm t} = 4.6 \text{ ns}$$

Thus the circuit is capable of producing 5 ns FWHM pulses from a laser operated in the pulse transmission mode. This was subsequently confirmed experimentally.

#### 4. ALTERNATIVE CIRCUIT FORMS

The basic avalanche chain may be used in a number of ways depending on the requirements. It can be used for normal Q switching, for operating a PTM laser or as a pulse selector (or gate).

#### 4.1 Q switch circuit

When used for Q switching, a single chain as shown in figure 7 is used. If the Q switch is connected to point 1, a DC bias is provided which is shorted to ground when the chain is fired. If connected to point 2, the Q switch has no bias and a fast pulse is obtained when the chain is fired. This would be used where it is desired to pulse open the Q switch, bias being provided optically.

#### 4.2 Cavity dump drive circuit

Considerable difficulty was experienced in devising a circuit combining two avalanche chains to operate independently within 100 ns of each other. With fast high voltage transients one might expect that firing one chain would induce the second to fire. I am indebted to Mr C. Flecker of this establishment (since retired) for the basic form of the successful circuit. This is shown in figure 8 in which the two transistor chains are again shown schematically as blocks. Chain A provides DC bias to the Q switch and when fired the bias is removed opening the Q switch. Chain B is capacitively coupled to the Q switch. When the capacitor is charged this side of the Q switch is held at ground potential by the resistive load. When chain B is fired a fast pulse is developed across the resistor, thus closing the Q switch rapidly. Note the resistive load removes the effect of the capacitive coupling as described in the preceding section.

The coupling capacitor used for chain B should be large compared to the Q switch capacitance as these form a capacitive voltage divider. The voltage appearing across the Q switch is

$$V_{q} = \frac{C_{q}}{C + C_{q}}$$

where  $\mathbf{C}_{\mathbf{q}}$  is the Q switch capacitance and  $\mathbf{C}$  is the coupling capacitor.

A high voltage diode as shown between chain B and the Q switch can help prevent fast transients from chain A interacting with chain B but is not essential.

This work was previously reported at the 1st Australian National Laser Conference, March 1978. Since then Davis et al(ref.13) have reported on a very similar circuit which was developed for pulse gating.

## 4.3 Pulse gating

If the Q switch connection to chain A is made between the resistor and capacitor, as for chain B, then no bias appears on the Q switch.

Firing of the two chains with a short delay between them now yields a square pulse which may be used to gate or select one pulse from a pulse train. This is the form of the circuit used by Davis et al.

#### 5. CONCLUSION

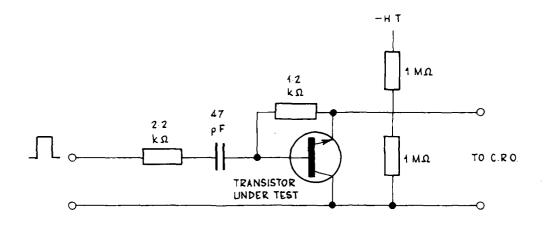
A very reliable avalanche transistor Q switch driver has been designed, based on the 2N5192 transistor. The double chain version has been successfully used to generate 5 ns FWHM pulses from a pulse transmission mode laser.

A single chain version has been used as a Q switch drive for a laser running at 168 Hz for well in excess of 100 hours. No life limitation is foreseen.

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(a) Basic test circuit

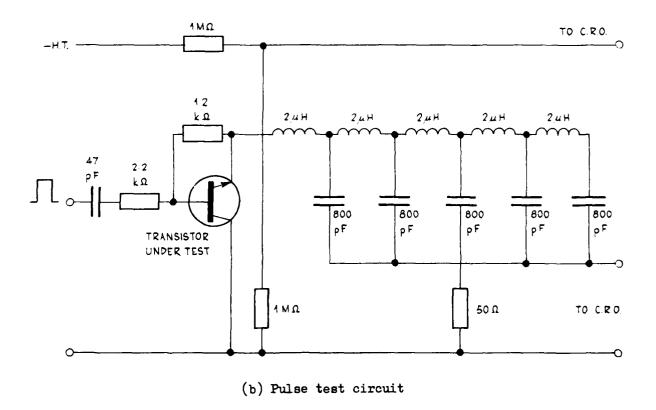


Figure 1. Test circuits for Avalanche transistors

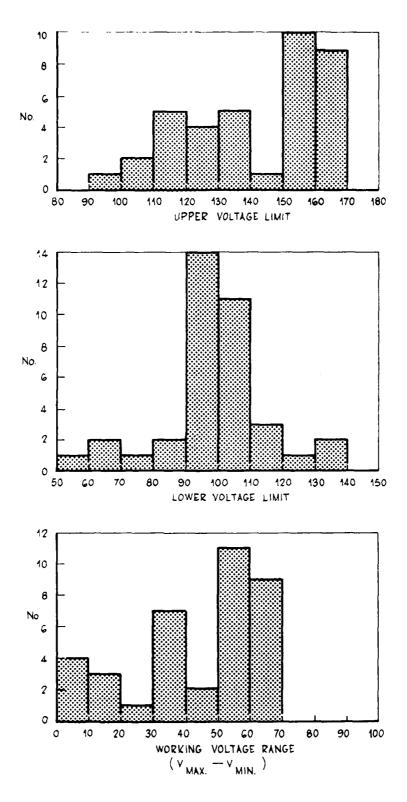


Figure 2. 2N2222 Avalanche characteristics

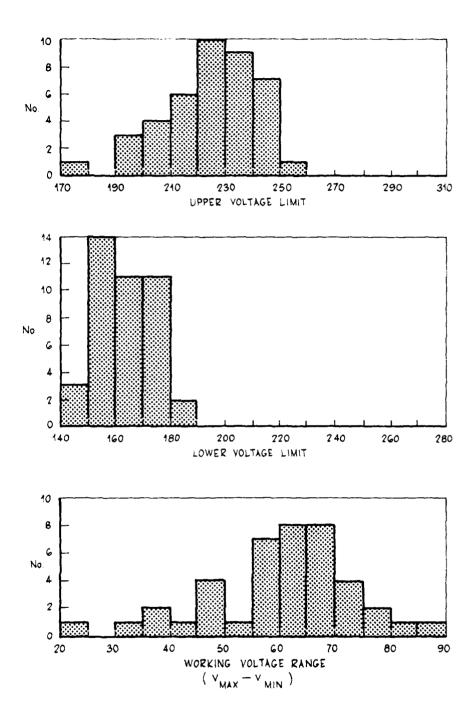


Figure 3. 2N5192 Avalanche characteristics

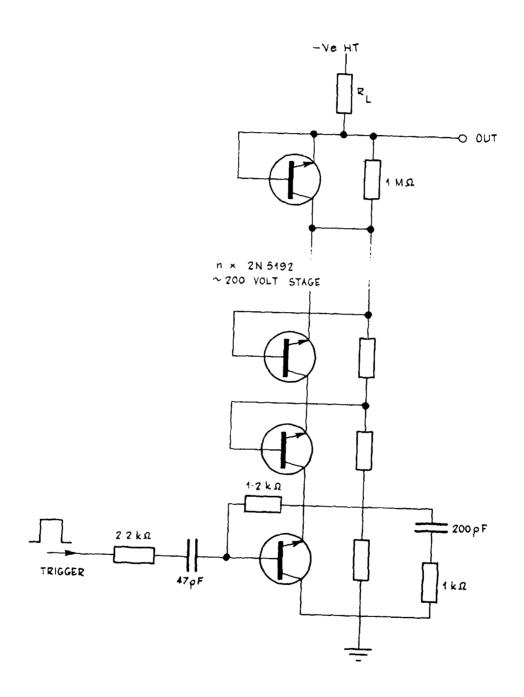


Figure 4. Avalanche transistor chain

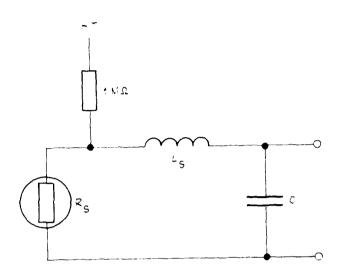
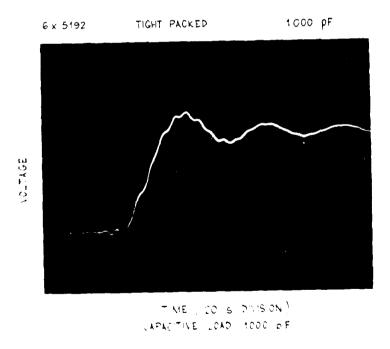


Figure 5. Equivalent circuit in ON state



righte 6. Voltage step for 6 transistor chain

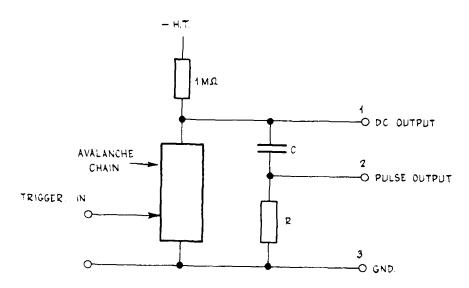


Figure 7. Circuit for pulse output

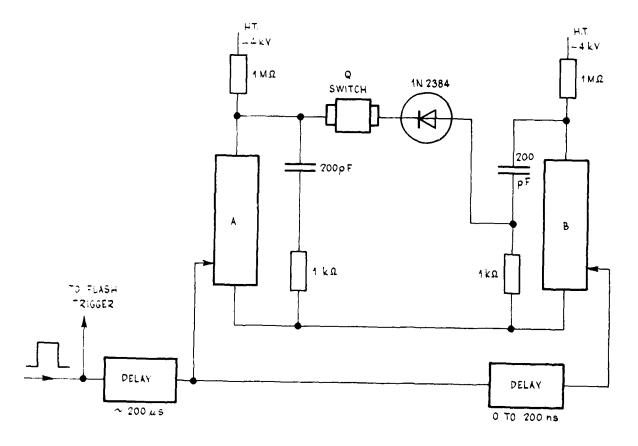


Figure 8. PTM Q switch drive circuit

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